CLAIMS

1. A printer comprising:

at least one laser driver;

a print control engine; and

a video controller, bidirectionally connected to the print control engine and the at least one laser driver via a system bus, having a video block that includes,

a direct memory access (DMA) controller,

a video processor,

a first data bus and control bus electrically connecting the DMA controller to the video processor,

a video signal generator, connected to the video processor,

a second data bus and control bus connecting the video processor to the video signal generator,

a frequency synthesizer connected to the video signal generator,

configuration registers bidirectionally connected to the DMA controller, video processor, the video signal generator and the frequency synthesizer, and

a data bus and control bus electrically connecting the DMA controller and the configuration registers to the system bus.

2. A printer, as defined in claim 1, the data bus and control bus including:

a third data bus and control bus electrically connecting the configuration registers to the system bus; and

a fourth data bus and control bus, electrically connecting the DMA controller to the system bus.

3. A printer, as defined in claim 1, wherein the video controller generates one pass of the one laser driver, the image generated being monochromatic.

4. A printer, as defined in claim 1, wherein the video controller generates multiple passes of the laser driver, the image generated containing four color planes.

5. A printer, as defined in claim 1, further comprising three color laser drivers, each connected to the video controller which has four video blocks, the image generated being an *in-line* color image.

6. A printer, as defined in claim 1, wherein:
the video controller further includes a second video block; and
a second laser driver connected to the video controller.

7. A printer, as defined in claim 6, wherein the video controller controls sharing the pass of the two laser drivers, the image generated being monochromatic.

8. A printer, as defined in claim 6, wherein the video controller generates multiple passes for each laser driver, the image generated containing four color planes.

9. A printer, as defined in claim 6, further comprising seven laser drivers, each connected to the video controller which has eight video blocks, the image generated being in-line color image.

10. A scanning control circuit comprising:
a direct memory access (DMA) controller;
a video processor;
a first data bus and control bus electrically connecting the DMA controller to the video processor;
a video signal generator, connected to the video processor;
a second data bus and control bus connecting the video processor to the video signal generator;
a frequency synthesizer connected to the video signal generator;
configuration registers bidirectionally connected to the DMA controller, video processor, the video signal generator and the frequency synthesizer; and
a data bus and control bus electrically connecting the DMA controller and the configuration registers to a system bus.

11. A scanning control circuit, as defined in claim 10, the data bus and control bus including:

a third data bus and control bus electrically connecting the configuration registers to the system bus; and

a fourth data bus and control bus, electrically connecting the DMA controller to the system bus.

12. A method for scanning a memory comprising:

determining a vertical direction for scanning the memory;

determining a horizontal direction for scanning the memory;

initializing the DMA address;

reading the data line;

updating the DMA address; and

repeating the steps of reading and updating.

13. A method, as defined in claim 12, wherein initializing comprises:

when the memory scan is top-to-bottom and left-to-right, the DMA Address is initialized to the Start Address;

when the memory scan is top-to-bottom and right-to-left, the DMA Address is initialized to the Start Address + data_per_line –1;

when the memory scan is bottom-to-top and left-to-right, the DMA Address is initialized to the Start Address -data_per_line*(linecount-1); and

when the memory scan is bottom-to-top and right-to-left, the DMA Address is initialized to the Start Address + (data_per_line*linecount) –1.

14. A method, as defined in claim 12, wherein updating comprises:

when the memory scan is top-to-bottom and left-to-right, the DMA Address is incremented to the DMA Address + (skips*data_per_line);

when the memory scan is top-to-bottom and right-to-left, the DMA Address is incremented to the DMA Address + ((2+skips) * data_per_line);

when the memory scan is bottom-to-top and left-to-right, the DMA Address is incremented to the DMA Address – ((2+skips)*data_per_line); and

when the memory scan is bottom-to-top and right-to-left, the DMA Address is incremented to the DMA Address – (skips*data_per_line).

15. A method, as defined in claim 12, wherein reading the data line includes,

setting a repeat counter to the number of desired repeats,

reading data at the DMA address,

horizontally updating the DMA address according to the direction of the horizontal read; and

when there is more data to be read, setting the DMA address to the line start address;

when there is more data to be read, repeating the steps of reading and horizontally updating.

16. A method, as defined in claim 15, wherein horizontally updating comprises incrementing the DMA address when the read is from left to right.

17. A method, as defined in claim 15, wherein horizontally updating comprises decrementing the DMA address when the read is from right to left.